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SmartDV to Exhibit at SemIsrael Expo, ICCAD China 2019

Will Feature Portfolio of SmartDV Verification IP,

Demonstrate Smart ViPDebug Protocol Debugger

SAN JOSE, CALIF. — November 6, 2019 — [SmartDV™ Technologies](#) will exhibit at [SemIsrael Expo 2019](#) in Airport City, Israel, November 19 and [ICCAD China 2019](#) November 21-22 in Nanjing, China.

At both events, SmartDV will showcase why it is the **Proven** and **Trusted** choice for Verification and Design Intellectual Property (IP), including new additions to its extensive and broad portfolio of protocols. SmartDV's latest VIP supports the TileLink chip-scale interconnect standard, an open-source, high-performance and scalable cache-coherent fabric for RISC-V based system-on-chip (SoC) designs, and Verilator, the free, open-source hardware description language (HDL) simulator.

In addition, SmartDV will demonstrate its Smart ViPDebug™, a visual protocol debugger that reduces debug time by rapidly identifying violations.

SemIsrael and ICCAD China attendees can schedule meetings to discuss SmartDV's Verification and Design IP or arrange for private demos of Smart ViPDebug at demo@smart-dv.com.

About SmartDV

[SmartDV™ Technologies](#) is the **Proven** and **Trusted** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Design and Verification IP supports simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification, RISC-V verification services. The result is **Proven** and **Trusted** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit [SmartDV](#) to learn more.

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