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SmartDV Delivers New Design IP for Video, Imaging, Entertainment System Protocols

Fast, Configurable Compliant Design IP Enables Users to Get to Market Quickly, Confidently

SAN JOSE, CALIF. — June 4, 2020 — SmartDV™ Technologies, the *Proven* and *Trusted* choice for Design and Verification Intellectual Property (IP), today delivered a series of video, imaging and entertainment system Design IP compliant with a variety of standard protocol specifications.

The new Design IP is available for:

- V-by-One, a high-speed serial video interface for HDTV
- VESA DSC (Display Stream Compression), a video compression and decompression standard
- HDCP 2.3 (High-Bandwidth Digital Content Protection) used to encrypt and authenticate digital signals for copyright-protected media, including movies, TV shows and audio
- HDMI CEC (Consumer Electronics Control), a feature of HDMI that allows devices connected to HDMI to be controlled by just one remote
- HDMI eARC (enhanced Audio Return Channel), an HDMI feature that enables high-quality digital audio to be sent back from the TV via HDMI
- CXP (CoaXpress), a high-speed imaging standard for serial transmission of video and still images
- SLVS-EC (Scalable Low Voltage Signaling with Embedded Clock), a highspeed serial interface scheme for image data transmission

"Our video, imaging and entertainment system protocol Design IP is part of our growing and extensive portfolio in support of our users," states Deepak Kumar Tala, SmartDV's managing director. "Each Design IP can be quickly customized to meet users' needs and has our commitment to high quality. That's why SmartDV is *Proven* and *Trusted* at more than 100 global organizations, including seven out of the top 10 semiconductor companies."

As with all SmartDV's Design IP solutions, its newest additions to video, imaging and entertainment system protocol Design IP enables users to get to market quickly and confidently. High performance and uniform quality are maintained across the entire portfolio of Design IP products. They are delivered in readable register transfer level (RTL) form, lint-proof, optimized for area and are highly configurable and reusable plugand-play design solutions.

SmartDV's standard and custom protocol Design IP is optimized for high performance, low power and minimum area/gate count. Rapid customization and first-to-market delivery of new industry protocols are achieved through SmartDV's proprietary automated compiler-based technology. Custom protocol or modifications to Design IP based on specific customer requests can be rapidly developed, validated and delivered after being fully tested on a field programmable gate array (FPGA) platform.

Availability and Pricing

The SmartDV video, imaging and entertainment system protocol Design IP is available now and backed by an experienced R&D team who work individually with each user installation. Advanced configuration and status reporting interfaces are

supplied, along with a comprehensive test suite that can be implemented in ASIC,

system-on-chip (SoC) or FPGA designs.

Pricing is available upon request.

Email requests for datasheets or more information should be sent to

sales@Smart-DV.com.

About SmartDV

SmartDV™ Technologies is the **Proven** and **Trusted** choice for Verification and

Design IP with the best customer service from more than 250 experienced ASIC and

SoC design and verification engineers. SmartDV offers high-quality standard protocol

Design and Verification IP for simulation, emulation, field programmable gate array

(FPGA) prototyping, post-silicon validation, formal property verification and RISC-V

CPU verification. Any of its Design and Verification IP solutions can be rapidly

customized to meet specific customer design needs. The result is *Proven* and *Trusted*

Design and Verification IP used in hundreds of networking, storage, automotive, bus,

MIPI and display chip projects throughout the global electronics industry. SmartDV is

headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

Connect with SmartDV at:

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