SmartDV™

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SmartDV Adds New Verification IP to Support OpenCAPI Standard
First to Market OpenCAPI Verification IP

SAN JOSE, CALIF –– June 25, 2019 –– SmartDV™ Technologies, the **Proven**

and **Trusted** choice for Verification Intellectual Property (IP), added new Verification IP

to support the OpenCAPI standard aimed at boosting the performance of data center

servers tasked with analyzing large amounts of data.

"OpenCAPI is an important new development that enables data to move through

the network faster and backed by the largest enterprise networking companies," states

Deepak Kumar Tala, managing director SmartDV. "Supporting this effort with a verified

Verification IP solution will accelerate OpenCAPI's adoption and acceptance."

The first commercially available OpenCAPI Verification IP is compatible with

OpenCAPI 3.0 and 3.1. It verifies OpenCAPI interfaces and includes an extensive test

suite that performs random or directed protocol tests to create a range of scenarios to

effectively verify the design under test.

SmartDV's OpenCAPI Verification IP is supported for all major verification languages and methodologies, including open verification methodology (OVM), universal verification methodology (UVM) and SystemC.

"The OpenCAPI Consortium is an open forum to manage the OpenCAPI specification and ecosystem, and we welcome the support of SmartDV and its exceptional verification solutions," remarks Myron Slota, OpenCAPI Consortium president.

SmartDV at ES Design West

SmartDV will feature its OpenCAPI Verification IP and its other smart Verification IP solutions in booth #2226 at ES Design West, Tuesday through Thursday, July 9-11, in the South Hall of San Francisco's Moscone Center as a co-located event at SEMICON West.

ES Design West attendees can schedule demonstrations through at:

demo@smart-dv.com

Pricing and Availability

The SmartDV OpenCAPI Verification IP is functional and shipping today.

Pricing is available upon request.

About SmartDV

SmartDV™ Technologies is the Proven and Trusted choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard or custom protocol Verification and Design IP is compatible with all verification languages, platforms and methodologies supporting all simulation, emulation and formal verification tools used in

a coverage-driven chip design verification flow. The result is ***Proven** and **Trusted***

Verification and Design IP used in hundreds of networking, storage, automotive, bus,

MIPI and display chip projects throughout the global electronics industry. SmartDV is

headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif. Visit

www.Smart-DV.com to learn more.

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