SmartDV™

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SmartDV Adds Support for MIPI I3C 1.1 Across Entire IP Portfolio
Verification and Design IP, Synthesizable Transactors, Post-Silicon Validation, SystemC TLM, Cycle-Accurate Models Compliant with new MIPI Specification

SAN JOSE, CALIF. — February 12, 2020 — SmartDV™ Technologies today announced its entire IP portfolio supports the new MIPI I3C® v1.1 utility and control bus specification designed to simplify integration and improve cost efficiencies for development of smartphone, wearable, high-performance server and automotive applications.

The portfolio of Verification and Design IP, synthesizable transactors for emulation and field programmable gate array (FPGA) prototyping, post-silicon validation and SystemC transaction level model (TLM) and cycle-accurate models, is fully compliant with the latest MIPI I3C v1.1 specification. SmartDV also adds support for the MIPI I3C host controller interface (HCI) 1.1 draft spec with its verification IP and master Design IP.

“The MIPI I3C v1.1 interface is a welcome update that benefits designers working on a wide spectrum of designs including mobile, automotive, high performance computing and others,” states Deepak Kumar Tala, chairman of SmartDV. “With its

flexibility to integrate inputs from multiple sensors of different types and a small footprint, MIPI I3C v1.1 promises to deliver on new applications and broader use cases. Our IP portfolio supports these features to meet design and verification requirements and help accelerate time-to-market delivery."

SmartDV's high-quality MIPI I3C 1.1 IP portfolio is cost-effective, configurable, interoperable and reusable for standard interfaces based on hardware verification languages (HVL) including SystemVerilog and SystemC. Simple to use and debug, each component comes with advanced commands, configurations and a status reporting interface. The IP can be customized to meet specific needs.

Announced January 15 by the MIPI Alliance, MIPI I3C v1.1 is a scalable, medium-speed, utility and control bus specification that connects peripherals to an application processor, streamlining integration and improving cost efficiencies. Relying on a lower number of pins and the smallest amount of PCB real estate compared with other bus solutions, MIPI I3C integrates mechanical, motion, biometric, environmental and any other type of sensor.

SmartDV will exhibit its IP portfolio at DVCon U.S. (Booth #304). Exhibits will be open during DVCon Expo and Reception Monday, March 2, from 5 p.m. until 7 p.m., Tuesday, March 3, and Wednesday, March 4, from 2:30 p.m. until 6 p.m. DVCon U.S. will be held at the DoubleTree Hotel in San Jose, Calif.

Availability and Pricing

The entire SmartDV MIPI and MIPI I3C 1.1 IP portfolio is available today.

Pricing is available upon request.

Email requests should be sent to demo@Smart-DV.com or sales@Smart-DV.com

About SmartDV

SmartDV™ Technologies is the ***Proven*** and ***Trusted*** choice for Verification and Design IP with the best customer service from more than 250 experienced ASIC and SoC design and verification engineers. Its high-quality standard protocol Design and Verification IP for simulation, emulation, field programmable gate array (FPGA) prototyping, post-silicon validation, formal property verification, RISC-V verification services can be rapidly customized to meet specific customer design needs. The result is ***Proven*** and ***Trusted*** Design and Verification IP used in hundreds of networking, storage, automotive, bus, MIPI and display chip projects throughout the global electronics industry. SmartDV is headquartered in Bangalore, India, with U.S. headquarters in San Jose, Calif.

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